Chip-Rate Adaptive Two-Stage Receiver for Scrambled Multirate CDMA Downlink

Adam R. Margetts and Philip Schniter
Dept. of Electrical Engineering
The Ohio State University
Columbus, OH
{margetta, schniter}@ee.eng.ohio-state.edu

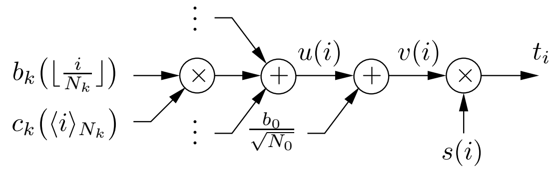

Fig. 1. Scrambled-CDMA transmitter model.

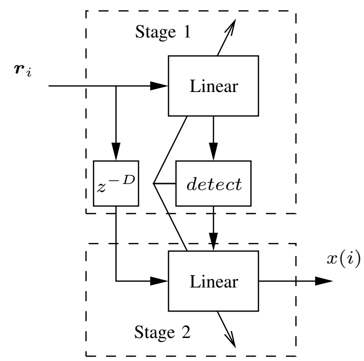

Fig. 2. Two-stage adaptive receiver block diagram.

***Abstract*— In this paper we propose an adaptive two-stage receiver for a scrambled multirate DS-CDMA downlink transmitted via synchronous orthogonal short codes and subjected to time- and frequency-selective multipath fading. The first stage of our two-stage receiver (described in a previous publication [1]) consists of adaptive FIR equalization generating tentative hard decisions. The decisions are fed-forward to the second stage for further processing via adaptive decision-feedforward equalization (DFFE) or adaptive inter-chip interference cancellation (ICIC). (The ICIC receiver was introduced in [2].) Here we detail the adaptive DFFE and ICIC structures, which are based on low-complexity decision-directed LMS. For further complexity reduction, the ICIC performs maximal ratio combining of only the ICIC branches corresponding to the largest channel taps. Since ICIC removes both pre- and post-cursor interference, it outperforms the DFFE.**

I. Introduction

In third generation mobile DS-CDMA systems, downlink multirate symbol streams are multiplexed using orthogonal short codes and then scrambled by a cell-specific long code prior to synchronous transmission, as shown in Fig.1. The multipath propagation channel creates inter-chip interference (ICI) in the received signal, which destroys the orthogonality among user codes, which in turn introduces multi-access interference (MAI) in the symbol estimates of matched-filter (MF) based detectors. Since the mobile terminals in these systems are cost- and power-limited, we desire a low-complexity solution.

The usual methods of multipath mitigation in CDMA (e.g., "blind minimum output energy" techniques [3]) rely on received signal cyclostationarity. In our application, however, the scrambling code destroys the cyclostationarity and so an alternative means of multipath mitigation is necessary. We focus on a two-stage receiver as shown in Fig. 2.

This work was supported in part by the Ohio Space Grant Consortium.

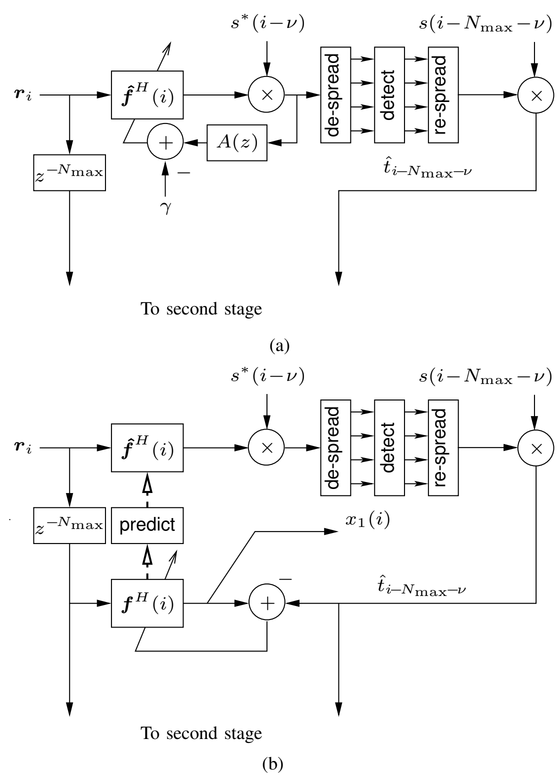

Fig. 3. Adaptive FIR equalizer first stage: (a) pilot trained AEAR-LMS, and (b) DD-LMS equalization.

A. First Stage

Frank and Visotsky [4] first proposed the use of a code-multiplexed pilot for equalizer adaptation in the scrambled CDMA downlink. Though Petre et al. [5] later extended this pilot-aided scheme to incorporate chip-fractional sampling, both [4], [5] update the equalizer at the symbol rate. Motivated by the potential for improved tracking performance, we considered a pilot-aided equalization algorithm, referred to as averaged-error average-regressor LMS (AEAR-LMS), that updates at the *chip* rate using an "error filtering" mechanism [1]. The mean transient response of the resulting algorithm corresponds to that of a third-order dynamical system (in contrast to standard LMS, which behaves as a first-order dynamical system [6]). Such higher-order LMS algorithms have demonstrated tracking performance superior to standard LMS [7].

The aforementioned pilot-aided scheme is intended for cold-start or loss-of-lock situations. When adequately reliable symbol estimates are obtained, the first stage switches to the decision-directed (DD) equalizer update algorithm , for which we assume all active user codes are known and employed in the equalizer update [1]. The chip-rate DD algorithm alleviates the MAI problem faced by the pilot-aided algorithm and consequently yields better performance. The receiver monitors pilot decision quality as a means of switching between AEAR-LMS and DD to update the FIR equalizer [1].

Whether in AEAR-LMS mode (see Fig.3(a)) or in DD mode (see Fig. 3(b)), the multiuser chip-rate sequence is detected and fed-forward to the second stage. In the block diagrams, ν denotes the system delay and $N_{\max}$ the spreading factor of the lowest rate user. Note that that any linear chip-rate equalization structure could serve as the first stage in our two-stage receiver.

B. Second Stage

In this paper, we present the details of two adaptive second-stage algorithms: decision feed-forward equalization (DFFE) and inter-chip interference cancellation (ICIC), which was introduced in [2]. The second stage of our receiver uses tentative decisions—produced by the first stage—for interference cancellation.

First-stage linear equalizers reduce MAI by re-orthogonalizing the chip-rate signal prior to the de-spreading operation. It has been noticed in [8], [9], however, that non-linear processing offers potential performance improvement. In [8], chips from a tentative decision of the current symbol are used as feedback in a decision feedback equalizer (DFE). However, ICI from only a single user is suppressed, and the algorithm is not amenable to adaptation. Our proposed algorithms are more reminiscent of [9], where the output of an FIR chip-level equalization stage is de-spread and soft-decoded to obtain estimates of all active users' symbol streams, which are then fed-forward to be re-spread and used as feedback information for re-processing the received signal via a chip-level DFFE stage. To reduce complexity and delay, our receiver foregoes the decoding step and instead feeds forward hard decisions.

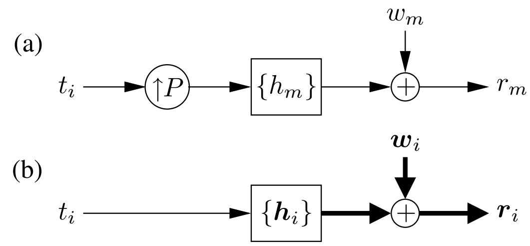

Fig. 4. Channel model at (a) chip-fractional-rate and (b) chip-rate.

We extend the DFFE concept from [9] to an *adaptive DFFE* and compare its performance to the *adaptive ICIC* structure. While DFFE eliminates post-cursor ICI, ICIC eliminates both post- and *pre*-cursor ICI in the received signal so that subsequent de-spreading removes all MAI in final symbol estimates. Adaptive ICIC employs a low-complexity LMS channel identification algorithm trained with chip-decisions that are fed-forward from the first stage.

II. System Model

Our transmitted signal model is illustrated in Fig. 1 with the following definitions. K denotes the number of users, N_k the k^{th} user's spreading gain, $\{b_k(n), n \in \mathbb{Z}\}$ the k^{th} user's symbol stream, $\{c_k(i), i = 0 \ldots N_k - 1\}$ the k^{th} user's short code (where i is the chip index), $\{u(i)\}$ the multiuser sequence, $\{v(i)\}$ the multiuser-plus-pilot sequence, $\{s(i)\}$ the scrambling sequence, and $\{t_i\}$ the transmitted sequence. In the sequel, we will use $\{\delta_i\}$ to denote the Kronecker delta sequence, $(\cdot)^*$ to denote the complex conjugate, $(\cdot)^T$ to denote the transpose, and $(\cdot)^H$ the Hermitian transpose.

Figure 4(a) describes the discrete-time chip-fractionally-spaced channel model using P samples per chip, where $\{h_m\}$ denotes the chip-fractional impulse response of the channel and pulse-shaping filters and where $\{w_m\}$ denotes additive circular-Gaussian channel noise. The chip-fractional received signal can be written as (see, e.g., [10] for a detailed development of this multirate fractionally-sampled channel representation):

$$r_m = \sum_{\ell} t_\ell h_{m-\ell P} + w_m. \tag{1}$$

A chip-spaced model follows from definition of the vectors $\boldsymbol{h}_i := \left[h_{iP+P-1}, \ldots, h_{iP}\right]^T$, $\boldsymbol{w}_i := \left[w_{iP+P-1}, \ldots, w_{iP}\right]^T$, and $\boldsymbol{r}_i := \left[r_{iP+P-1}, \ldots, r_{iP}\right]^T$, as in Fig. 4(b). Then

$$\boldsymbol{r}_i = \sum_{\ell=0}^{L_h} \boldsymbol{h}_\ell \, t_{i-\ell} + \boldsymbol{w}_i, \tag{2}$$

Since the DFE feed-forward filter employs a window of L_f+1 chip-spaced samples, we define $\boldsymbol{r}(i) := \left[\boldsymbol{r}_i^T, \ldots, \boldsymbol{r}_{i-L_f}^T\right]^T$, $\boldsymbol{t}(i) := \left[t_i, \ldots, t_{i-L_h-L_f}\right]^T$, $\boldsymbol{w}(i) := \left[\boldsymbol{w}_i^T, \ldots, \boldsymbol{w}_{i-L_f}^T\right]^T$, and the block-Toeplitz matrix

$$\boldsymbol{H} := \begin{bmatrix} \boldsymbol{h}_0 \cdots \boldsymbol{h}_{L_h} & & \\ & \ddots & \ddots \\ & & \boldsymbol{h}_0 \cdots \boldsymbol{h}_{L_h} \end{bmatrix},$$

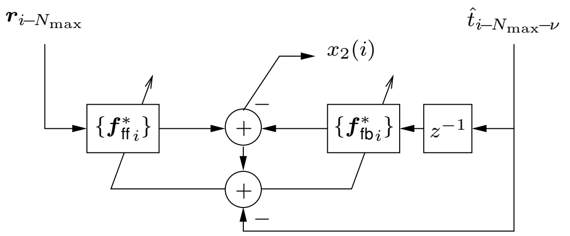

Fig. 5. Adaptive chip-rate DFFE.

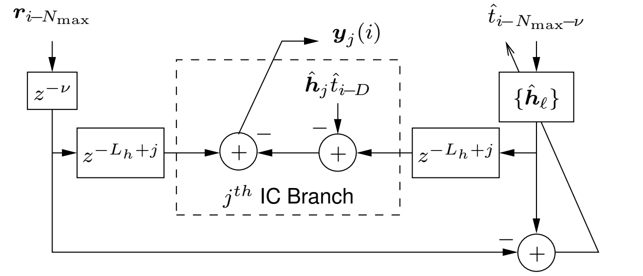

Fig. 6. Adaptive ICIC branch corresponding to cursor j.

so that

$$\boldsymbol{r}(i) \;=\; \boldsymbol{H}\boldsymbol{t}(i)+\boldsymbol{w}(i). \tag{3}$$

For simplicity of presentation, the system model (2) assumes that the channel is fixed, which is approximately true over short time periods. The simulations, however, are conducted using time- and frequency-selective channels.

We make the following assumptions about our system.

(A1) Circular, i.i.d., zero-mean, PSK scrambling $\{s(i)\}$.
(A2) Multirate orthonormal Walsh codes.
(A3) Constant pilot at user index $k=0$.
(A4) Circular, independent, zero-mean user symbols.
(A5) Zero-mean, circular, white, Gaussian noise $\{w_m\}$ with variance σ_w^2, independent of $\{b_k(n)\}$ and $\{s(i)\}$.

III. Decision Feedforward Equalization

In this section we propose an adaptive chip-rate DFFE structure for the second stage of our receiver. The DFFE is illustrated in Fig. 5, where $\boldsymbol{f}_{\mathsf{ff}}$ denotes the feed-forward filter (FFF), $\boldsymbol{f}_{\mathsf{fb}}$ denotes the feed-back filter (FBF), and $N_{\max}$ denotes the lowest-rate user's spreading gain. We use the term DFFE rather than DFE because decisions are *fed forward* from, rather than *fed back* to, the first-stage. In the following discussion, we use *cursor* to denote the overall delay of the channel/feed-forward-filter and denote it by ν. Due to the relative delay between $\{\boldsymbol{r}_{i-N_{\max}}\}$ and $\{\hat{t}_{i-N_{\max}-\nu}\}$, the overall delay of the first-stage channel/equalizer is also ν.

In conventional DFE, post-cursor interference cancellation is accomplished by subtracting FBF-filtered past-decisions at the decision-device input. In a multirate CDMA system, however, the decision-making process incurs a delay of $N_{\max}$ chips, which can be much greater than the delay spread of the channel. In this case, the feedback signal would not cancel interference present at the decision-device input and the benefit of DFE would vanish. As an alternative, tentative decisions could be fed-*forward* from a previous stage to replace this "DFE feedback" signal, as shown in Fig. 5. Final bit decisions are made by de-scrambling and de-spreading $x_2(i)$, the output of the DFFE. The effectiveness of DFFE post-cursor interference cancellation, however, is not related to DFFE output signal quality but rather the quality of the tentative decisions produced by the previous-stage; this is an important difference between DFFE and DFE.

LMS adaptation is readily applied to update the DFFE feed-forward and feed-back filter weights. [Note from (A1) and (A4) that $\{t_i\}$ is stationary.] The overall system delay is $N_{\max}+\nu$ and, defining $\tilde{\boldsymbol{f}}(i) := \left[\boldsymbol{f}_{\mathsf{ff}}^T(i), \boldsymbol{f}_{\mathsf{fb}}^T(i)\right]^T$, $\hat{\boldsymbol{t}}(i) := \left[\hat{t}_i, \ldots, \hat{t}_{i-L_b+1}\right]^T$, and $\tilde{\boldsymbol{r}}(i) := \left[\boldsymbol{r}^T(i), \hat{\boldsymbol{t}}(i-\nu-1)^T\right]^T$, where L_b is the feedback-filter length, the adaptive step-size LMS [11] update equations are:

$$
\begin{aligned}
e(i) &= \tilde{\boldsymbol{f}}^H(i)\tilde{\boldsymbol{r}}(i-N_{\max}) - \hat{t}(i-N_{\max}-\nu), && (4)\\
\boldsymbol{\psi}(i+1) &= \left[\boldsymbol{I} - \mu_i \tilde{\boldsymbol{r}}(i-N_{\max})\tilde{\boldsymbol{r}}^H(i-N_{\max})\right]\boldsymbol{\psi}(i) \\
&\quad -\tilde{\boldsymbol{r}}(i-N_{\max})e^*(i), && (5)\\
\mu_{i+1} &= \mu_{i+1} - \zeta \Re\left\{\boldsymbol{\psi}^H(i)\tilde{\boldsymbol{r}}(i-N_{\max})e^*(i)\right\}, && (6)\\
\tilde{\boldsymbol{f}}(i+1) &= \tilde{\boldsymbol{f}}(i) - \mu_i \tilde{\boldsymbol{r}}(i-N_{\max})e^*(i). && (7)
\end{aligned}
$$

For completeness, we state the well-known MMSE-DFE equalizer solution given perfect channel knowledge (denoted in the simulations by Max-SINR+DFE) [12]:

$$
\begin{aligned}
\boldsymbol{f}_{\mathsf{ff}}^{(\mathsf{MMSE})} &= \left(\boldsymbol{H}(\boldsymbol{I}-\boldsymbol{M}^T\boldsymbol{M})\boldsymbol{H}^H + \tfrac{\sigma_w^2}{\sigma_t^2}\boldsymbol{I}\right)^{-1}\boldsymbol{H}\boldsymbol{e}_\nu, && (8)\\
\boldsymbol{f}_{\mathsf{fb}}^{(\mathsf{MMSE})} &= -\boldsymbol{M}\boldsymbol{H}^H\boldsymbol{f}_{\mathsf{ff}}^{(\mathsf{MMSE})}, && (9)
\end{aligned}
$$

where $\boldsymbol{M} = \left[\boldsymbol{0}_{L_b\times\nu+1} \quad \boldsymbol{I}_{L_b\times L_b} \quad \boldsymbol{0}_{L_b\times L_h+L_f-\nu-L_b}\right]$, and $\boldsymbol{e}_\nu$ is a unit vector of zeros with a one in the ν^{th} position $0 \le \nu \le L_h + L_f + 1$.

IV. Inter-Chip Interference Cancellation

The ICIC uses chip-decisions fed forward from the first stage to cancel both pre- *and* post-cursor interference in the received signal. While DFFE employed a single cursor "ν," ICIC diversity-combines statistics from multiple cursors "j" where $j \in \{0,\ldots,L_h\}$. In ICIC, ν will still refer to the overall delay of the first-stage channel/equalizer. To recover the energy of the desired chip t_{i-D} using cursor choice j, where $D := N_{\max}+\nu+L_h$, the tentative sequence $\{\hat{t}_{i-N_{\max}-\nu}\}$ is filtered using the impulse response $\{\hat{\boldsymbol{h}}_0,\ldots,\hat{\boldsymbol{h}}_{j-1},\boldsymbol{0},\hat{\boldsymbol{h}}_{j+1},\ldots,\hat{\boldsymbol{h}}_{L_h}\}$ and subtracted from the received signal $\{\boldsymbol{r}_{i-N_{\max}}\}$. Equivalently, we could filter using the complete impulse response $\{\hat{\boldsymbol{h}}_\ell\}_{\ell=0}^{L_h}$ and subtract out the effect of the unwanted tap $\hat{\boldsymbol{h}}_j$, as in Fig. 6. The output of the j^{th} ICI-cancellation branch is

$$
\begin{aligned}
\boldsymbol{y}_j(i) &= \boldsymbol{r}_{i-D+j} - \sum_{\ell\neq j}\hat{\boldsymbol{h}}_\ell\hat{t}_{i-D+j-\ell}, && (10)\\
&= \boldsymbol{h}_j t_{i-D} + \sum_{\ell\neq j}\left(\boldsymbol{h}_\ell t_{i-D+j-\ell} - \hat{\boldsymbol{h}}_\ell\hat{t}_{i-D+j-\ell}\right) \\
&\quad + \boldsymbol{w}_{i-D+j}. && (11)
\end{aligned}
$$

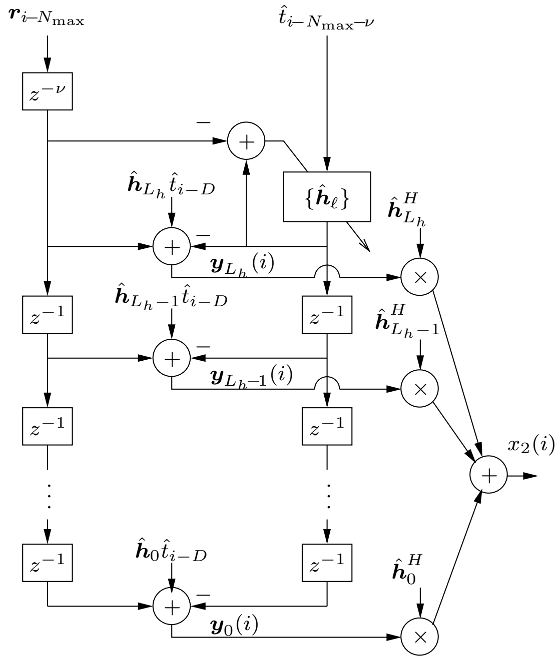

Fig. 7. Adaptive ICIC with maximum-ratio combining.

If perfect channel-tap estimates and correct bit-decisions are available; i.e., $\hat{\boldsymbol{h}}_\ell = \boldsymbol{h}_\ell \ \forall \ell$ and $\hat{t}_k = t_k \ \forall k \neq i-D$, then (11) implies $\boldsymbol{y}_j(i) = \boldsymbol{h}_j t_{i-D} + \boldsymbol{w}_{i-D+j}$, in which case we have an interference-free estimate of the transmitted chip sequence. Since it is desirable to take advantage of the diversity provided by the channel, the ICIC branches corresponding to different cursors are maximum-ratio combined to form the ICIC output $x_2(i)$ (see Fig. 7). Assuming perfect ICI cancellation and perfect channel estimates,

$$x_2(i) = \|\boldsymbol{h}\|^2 t(i-D) + \sum_{j=0}^{L_h} h_j^* w(i-D+j), \quad (12)$$

where $\boldsymbol{h} = \left[\boldsymbol{h}_0^T, \ldots, \boldsymbol{h}_{L_h}^T\right]^T$. The quantity $x_2(i)$ in (12) can be recognized as the (ICI-free) matched-filter output in AWGN. Final bit decisions can then be obtained by de-spreading $x_2(i)$, where MAI would be perfectly removed due to the code-orthogonality assumption (A2). While, in practice, channel estimation errors and tentative decision errors will degrade the quality of $x_2(i)$, our simulation results suggest that second-stage ICIC processing results in a net benefit at all SNRs.

The channel estimate of the ICIC can be made adaptive via LMS update using the tentative decisions as training:

$$\boldsymbol{e}(i) = \hat{\boldsymbol{H}}^T(i)\,\hat{\boldsymbol{t}}(i-N_{\max}-\nu) - \boldsymbol{r}_{i-N_{\max}-\nu} \quad (13)$$

$$\hat{\boldsymbol{H}}(i+1) = \hat{\boldsymbol{H}}(i) - \mu \boldsymbol{e}^T(i) \otimes \hat{\boldsymbol{t}}^*(i-N_{\max}-\nu). \quad (14)$$

where $\otimes$ denotes the Kronecker product and $\hat{\boldsymbol{H}}(i) = [\hat{\boldsymbol{h}}_0(i), \ldots, \hat{\boldsymbol{h}}_{L_h}(i)]^T$.

We can take advantage of sparse channels, i.e., those with only a few significant multipaths, by making the ICIC combining operation itself sparse; only the branches corresponding to the largest channel coefficients need to be combined to form $x_2(i)$.

V. Simulations

In the simulations we assume a 1/2-chip spaced, 1/2-loaded, synchronous DS-CDMA downlink consisting of one user at each of the following spreading factors: $\{4, 8, 16, 32, 64, 128, 256\}$. Users transmit BPSK symbols with equal power $\{P_k\}_{k=1}^K = 1$ and the pilot has spreading factor of 256 with power $P_0 = 4$. SNR-per-user is defined as P_k/σ_w^2. A "typical-urban" Rayleigh-fading channel [13] is used where channel rays have the power-delay profile that spans approximately 2 μs. The chipping rate is 3.84 Mcps, the carrier frequency is 2 GHz, and the square-root raised-cosine chip waveform has excess bandwidth 0.22. Except where noted, the plots show uncoded BER performance averaged across all users. As a lower limit to uncoded BER, the plots show the matched filter (single-user) bound (MFB) for spreading factors 4 (dashed) and 256 (solid)—see [14] for the details of computing the MFB for scrambled CDMA.

Fig. 8 shows the performance of the first stage. The adaptive rake employs pilot-based channel estimation in which de-scrambled pilot-matched-filter outputs were averaged using single-pole filters whose pole locations were BER-optimized through simulation. The equalizers span 25 chips (50 taps) with system delay $\nu = 21$, and the adaptive rake spans the entire 28-chip channel delay spread (i.e., 56 taps). The AEAR-LMS (AEAR) algorithm [1] outperforms the adaptive rake at moderate to high SNR, and with switching to DD mode (DD) enabled, BER is significantly reduced at all SNR levels. The max-SINR (max-SINR) receiver maximizes the signal to interference plus noise ratio (SINR) in the symbol estimates. Unlike the adaptive algorithms, the max-SINR receiver assumes perfect knowledge of the time-variant channel.

Fig. 9 and Fig. 10 show the performances of two-stage receivers with DFFE and ICIC as the second stage, respectively. The ICIC receiver offers superior performance due to its ability to cancel both pre- and post-cursor interference. At 16 dB SNR, the ICIC receiver reduces BER by more than an order of magnitude over first-stage processing. The Max-SINR+DFFE and Max-SINR+ICIC curves show performance with perfect channel knowledge for both stages. Sparse ICIC performance is shown in Fig. 11, where ICIC combines only the L largest channel taps. Performance with $L = 15$ is nearly the same as with $L = L_h$ (i.e., a non-sparse implementation).

VI. Conclusions

We proposed a two-stage adaptive receiver for the scrambled multirate CDMA downlink with a FIR equalizer first stage and an ICI-canceling second stage. We found, through simulation, that the two-stage adaptive ICIC receiver outperforms single-stage and two-stage DFFE receivers. The superior performance is attributed to ICIC's ability to attenuate both pre- and post-cursor ICI in the received chip-rate signal.

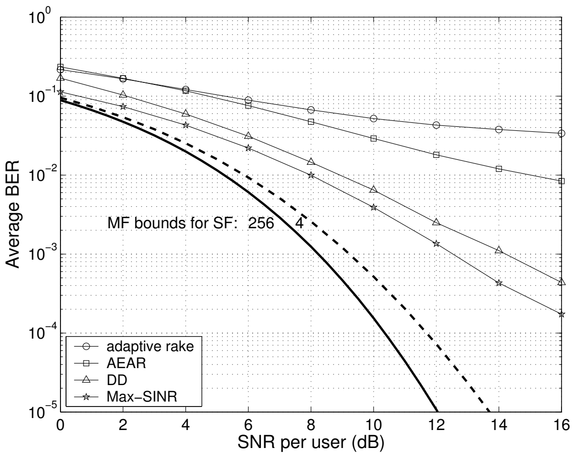

Fig. 8. Average uncoded BER vs SNR for one-stage receiver.

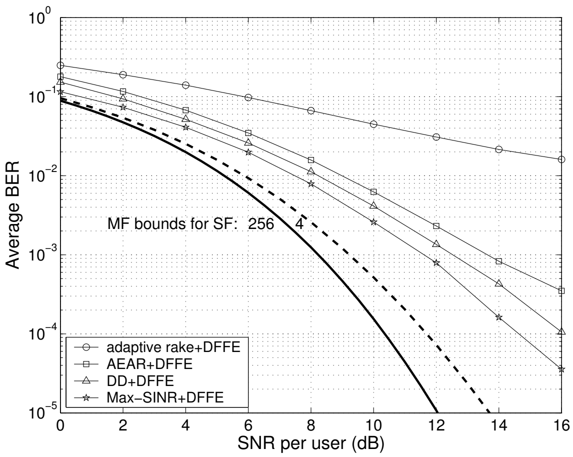

Fig. 9. Average uncoded BER vs SNR for two-stage receiver with DFFE second stage.

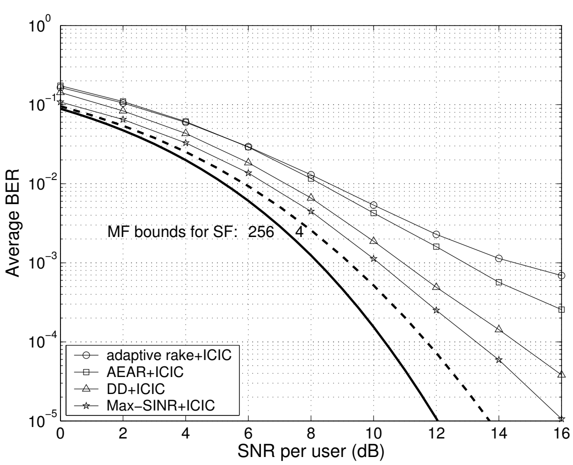

Fig. 10. Average uncoded BER vs SNR for two-stage receiver with ICIC second stage.

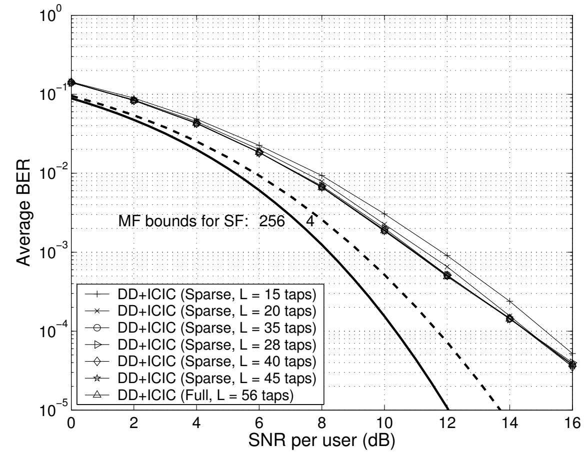

Fig. 11. Average uncoded BER vs SNR for *sparse* ICIC.

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